

Inventor

**Method for Attaching a Semiconductor Die to a Substrate**

**Technical Field**

This invention relates to semiconductor manufacturing and packaging.  
5 Particularly, it relates to a method for attaching a semiconductor die directly to an organic substrate such as a printed circuit board.

**Background of the Invention**

(In the final stages of semiconductor manufacturing, a semiconductor "chip" or die is typically enclosed within a sealed package. The primary purpose of the semiconductor package is to provide a lead system for electrically and mechanically connecting the circuits on the die to a supporting structure such as a printed circuit board (PCB). Without the lead system, electrical connections to the die are made difficult by the fragile structure of the die face. The package also provides physical and environmental (e.g., moisture, chemical) protection and serves to dissipate heat from the die.

The conventional semiconductor packaging process starts by securing the die to a mounting paddle of a metal lead frame with a suitable adhesive. Electrical connections between bond pads on the face of the die and connections on the leads are then made using fine bond wires. A protective coating may be applied to portions of the die, bonding wires, and lead frame. The package is then encapsulated in a plastic or ceramic material from which the leads extend outwardly therefrom. The package may be trimmed and the leads formed to achieve the desired configuration.)

25 A variation of conventional packaging is known as lead-on-chip (LOC) packaging. LOC differs in that the LOC lead frame has no mounting paddle. The leads of the lead frame attach directly to the face of the die and support the die

5 during the encapsulation process. LOC results in improved heat transfer and shorter bond wire length.

10 While both of these packaging methods have proven reliable, drawbacks exist. First, the encapsulation process adds cost to the finished semiconductor package. In addition, the equipment necessary for encapsulation is highly specialized and expensive. Finally, an encapsulated die is substantially larger and heavier than the die in its unpackaged state. As demand for smaller, more powerful electronic devices grows, semiconductor manufacturers are constantly seeking to increase semiconductor population within a given volume. Accordingly, the size of the semiconductor package becomes a significant concern.

15 To overcome these problems, alternatives to standard packaging have emerged. One such alternative is to eliminate the encapsulant and metal lead system altogether and attach the die directly to a PCB substrate. The resulting "chip-sized package" (CSP) may, in turn, may be attached through various means to other components including other printed circuit boards. By eliminating the die package and metal lead system, the die has a significantly smaller footprint (and volume). Thus, denser mounting may be achieved.

20 Bare die attachment to a PCB substrate generally involves first mounting the die to a die attach area on the substrate. The bond pads on the die face may then be wire bonded to connection points on the substrate using gold or aluminum wire. Or, as an alternative to wire bonding, the die may have a series of solder bumps on its face, which, when placed face down, contact connection points on the substrate. Heat or ultrasonic energy may be used to secure the solder bumps to the substrate. Since this process (often referred to as "flip chip bonding") requires specialized equipment, wire bonding remains the predominant and economically preferred

25 method of die interconnection.

Typically, an encapsulant is applied to the bond wire area to protect the bond wires and their connections. However, this encapsulant is typically a liquid material

or "glob-top" applied locally and, thus, its application is not as complex or as costly as conventional encapsulation. Likewise, glob-top provides negligible volumetric increase to the die and substrate.

Since the CSP package has no metal lead system, an alternative method of external electrical and mechanical connection must be provided. The package may, for example, include a fine-pitch "ball grid array" or BGA. A BGA is an array of solder bumps or balls on a side of the PCB opposite the die attach area. Each ball is electrically connected through a conductive trace in the substrate to a wire bond connection point which, in turn, is wire bonded to the die. To mount the BGA package, the solder bumps contact conductive points on the receiving component and heat is applied to reflow the bumps. Other connection methods such as a "pin grid array" or PGA may be used. A PGA has a series of pins extending outwardly from the substrate rather than solder bumps. The pins are mechanically received in apertures on the receiving component. Accordingly, with CSP applications, the substrate itself must incorporate the lead system for electrical connection to the die.

While CSP reduces the bulky footprint common with conventional die packaging, attaching dice directly to PCBs introduces problems. One area of particular concern is the adhesive used to attach the die. The adhesive must physically secure the die and firmly retain it during all subsequent manufacturing operations (e.g., wire-bonding, glob-top curing, soldering). (Generally speaking, die attach adhesives fall into one of two categories: tape and paste.) In LOC packaging, adhesive tape or film is sometimes used to secure the die to the metal lead frame. This tape is typically a thermoplastic material such as polyimide film requiring high temperature processing. Often, lamination of LOC tape requires temperatures ranging from 325 - 400 deg C. While the lead frame and other components involved in conventional packaging are capable of this high thermal processing, organic substrates are not. Specifically, the substrate may severely outgas and degrade at temperatures well below 325 deg C. For this reason, paste or resin adhesives

having substantially lower processing temperatures have been developed for use with organic substrates. While satisfactory in addressing the thermal processing issue, paste adhesives have inherent drawbacks.

For example, due to the viscous properties of the paste, it tends to "bleed" outwardly from where it is applied. In some instances, the paste may migrate to the wire bond area (or other non-solder masked area). When this occurs, the package is typically rejected. Careful manufacturing control is thus necessary to prevent paste bleed.

Another problem associated with the viscous properties of paste adhesives is bond line thickness and bond area coverage. Without maintaining an even paste thickness, the die may seat in a non-parallel orientation relative to the substrate. When this occurs, damage to the edge of the die and/or the substrate may occur.

A related problem caused by reduced bond line thickness concerns the glob-top or over-mold material. Such materials may contain filler particles that can contact and damage the die face. Increased bond line thickness has been found to reduce this occurrence. However, as discussed above, bond line thickness is difficult to control with paste. Simply adding more paste generally results in increased paste displacement rather than greater bond line thickness.

Yet another problem related to the viscous characteristics of the paste is voiding. Due to the consistency of the paste and the inclusion therein of solvent diluents, voids may form during paste dispensing. These voids increase outgassing during subsequent thermal processing. Outgassing may adversely affect wire bond effectiveness and glob-top adhesion.

Still yet another drawback to paste adhesives is the limitations inherent in dispensing the paste. Specifically, paste is limited by filler size and distribution to accomplish certain flow characteristics necessary for dispensing. Because of the method in which paste is dispensed, the rheological properties of the paste must fall within certain defined limits. Particularly, the filler material, size, distribution, and

percentage within the paste is critical to provide effective flow of the adhesive.

Accordingly, filler must be selected for its rheology characteristics rather than for its adhesive or mechanical properties.

Paste also requires curing. The introduction of heat into the lamination process may create thermal stresses into the bond line due to differing coefficients of thermal expansion (CTE) between the adhesive and the adherents. This may weaken the adhesive bond or warp the substrate.

Another problem with paste adhesive in die attach applications is that it is not in-line processable. Paste must be dispensed from above the substrate.

Currently available die attachment machines, however, attach the die from beneath the substrate. Therefore, the substrate must be inverted after the paste is dispensed and before the die is attached. This adds another step in the manufacturing process which further increases production time and cost.

Thus, there are unresolved issues, some of which are enumerated above, with present die attachment technology. Specifically, an improved method for attaching dice directly to organic substrates is needed.

#### Summary of the Invention

An improved method of attaching a semiconductor die to an organic substrate and an improved semiconductor package are provided herein. The package comprises a semiconductor die, an organic support structure, and an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape has an adhesive such as pressure sensitive adhesives, thermoplastic adhesives, thermoset adhesives or the like. The organic support structure may be a printed circuit board. A method of attaching a semiconductor die to an organic support structure comprises selecting a two-sided adhesive tape having an adhesive such as a pressure sensitive adhesive, thermoplastic adhesive, thermoset adhesive, or the like; affixing a first side of the two-sided adhesive tape to a surface

of the organic support structure; and affixing a face of the semiconductor die to a second side of the adhesive tape.

The adhesive tape may be a single adhesive layer or a multi-layer film. In one embodiment, the adhesive tape comprises a first adhesive layer adjacent to the organic support structure, a second adhesive layer adjacent to the semiconductor die, and a carrier layer intermediate the first and second adhesive layers. The first adhesive layer may have a first coefficient of thermal expansion substantially identical to that of the support structure. Similarly, the second adhesive layer may have a second coefficient of thermal expansion substantially identical to that of the semiconductor die. The intermediate carrier layer may be a polyimide film. The organic support structure may additionally comprise a feature that permits interconnecting the package to other electronic components. In one embodiment, the interconnecting feature is a BGA.

Another method for attaching a die to an organic support structure is disclosed generally comprising affixing a first side of a two-sided adhesive tape to the surface of the organic support structure; elevating the temperature of the tape to activate the adhesive; applying pressure to the tape and organic support structure to laminate the first side of the adhesive tape to the organic support structure; affixing a face of the semiconductor die to the second side of the adhesive tape; elevating the temperature of the tape to activate the adhesive; and applying pressure to the die and organic support structure to laminate the second side of the adhesive tape to the die.

Furthermore, the bond pads may be electrically connected to the lead connections on the organic support structure. An encapsulating material may then be formed around portions of the die and organic support structure. In one embodiment, the encapsulating material is a curable glob-top occupying negligible volume.

The support structure may be trimmed to form a BGA package comprising the die and the organic support structure, with the encapsulating material protecting the bond pads, bond wires and lead connections.

5 The BGA package may be interconnected to a receiving electronic component such as a system PCB. The finished BGA package is smaller and more economical to produce than conventional encapsulated packages. Additionally, the adhesive tape described herein is advantageous over the paste adhesives currently used to attach dice to organic substrates.

10 **Brief Description of the Drawings**

The invention described herein will be further characterized with reference to the drawings, wherein:

15 Figure 1 is an enlarged side view of a semiconductor package of the present invention;

Figure 2 is an exploded perspective view of a one embodiment of the PCB substrate showing a plurality of die receiving areas;

Figure 3 is a plan view of a semiconductor die attached to a PCB substrate according to one embodiment of the present invention;

20 Figure 4 is an enlarged side view of one embodiment of the adhesive tape of the present invention;

Figure 5a-5f are schematic side elevation views illustrating the steps for packaging a semiconductor die according to one embodiment of the present invention; and

25 Figure 6 is a diagrammatic view of a system having a memory device incorporating a semiconductor package according to one embodiment of the present invention.

### Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Generally, the present invention is directed to an improved semiconductor package and an improved method for attaching a semiconductor package to a support structure. Particularly, the invention is directed to support structures that are incompatible with conventional thermal processing operations, i.e., substrates that may degrade at lower temperatures than conventional substrate materials. This category of support structures will be hereinafter referred to generally as organic support structures/substrates and specifically as printed circuit board (PCB) substrates. Those skilled in the art, however, will realize that other substrate materials are also within the scope of the invention.) Thus, references to organic support structures and PCBs are not intended to limit the scope of the invention.

Referring generally to Figure 1, a die 10 and a PCB substrate 12 are shown. The die 10 is generally a flat, rectangular device having a plurality of integrated circuits (not shown) formed on a side of the die. In one embodiment, the circuits are disposed on a face side 14. A plurality of center bond pads 16 are located on the face 14 and form the electrical connections to the die's integrated circuits. While shown with circuits and bond pads on the face 14, those skilled in the art will realize that the circuits and bond pads may be disposed on a back side 15 of the die. In the latter case, apertures (not shown) through the die permit electrical connection to the die's integrated circuits.

Referring now to Figure 2, the PCB 12 may be a flexible board or film having side rails 18, 20 to support the substrate during manufacture. In one

embodiment, the substrate comprises a BT (bismaleimide triazine) resin core. In order to increase manufacturing efficiency, the substrate 12 may be a continuous sheet or film capable of accommodating a plurality of dice. A series of indexing openings 22 may be used to aid automation machinery. The PCB 12 additionally 5 has a first side 24 having a die attach area 26 and a second side 28 (best shown in Figure 3) having a plurality of lead connection pads 30. Still referring to Figure 2, the die attach area 26 is rectangular and substantially identical in size to the die 10. The die attach area may be slightly recessed in the substrate or it may be formed on 10 the substrate surface. A rectangular aperture 32 is formed through the center of the die attach area 26. A slot 33 separates each die attach area from the next. The purpose of the aperture 32 and slot 33 will become apparent shortly.

Referring to Figure 3, the second side 28 of the PCB 12 comprises a ball grid 15 array (BGA) 34. The BGA permits electrical and mechanical interconnection of the die 10 and substrate 12 to other electronic components including other circuit boards. The BGA 34 comprises an array of solder bumps or balls 36 (which may be formed during a subsequent manufacturing operation) connected by traces to the connection pads 30. While a BGA is represented in this embodiment, other connection methods (e.g., mechanical) are also considered to be within the scope of 20 the invention. The connection pads 30, in turn, are connected by a series of fine bond wires 38 to the bond pads 16 (best shown in Figure 1). Thus, the BGA 34 provides a lead system for electrical connection to the integrated circuits on the die face 14.

Unlike a metal lead frame, the PCB 12 is an organic material. As such, it is incapable of withstanding the high thermal processing temperatures often associated 25 with conventional (i.e., lead frame) packaging. Accordingly, thermal processing temperatures must remain relatively low.

As best viewed in Figure 1, an adhesive tape 40 lies intermediate to the die 10 and PCB 12. The adhesive tape 40, which is shown in detail in Figure 4, is a

two-sided dielectric material having a first side 42 that adheres to the die attach area 26 and a second side 44 that adheres to the die 10. In one embodiment, the adhesive tape 40 comprises two strips, one on each side of the aperture 32. (The tape 40 may be a single polymeric adhesive layer or, alternatively, it may be a multi-layer material as shown in Figure 4.) With the latter, the tape comprises a first adhesive layer 46 proximate the substrate 12, a second adhesive layer 48 proximate the die 10, and an intermediate layer 50. Other single and multi-layered tapes are also considered to fall within the scope of the invention.

*Subj* The adhesive layer(s) 46, 48 may be responsive to heat, pressure, or both. In one embodiment, the heat responsive component is a thermoset material. The thermoset material may be a "B-stageable" material (i.e., having an intermediate stage in which the material remains wholly or partially plastic and fusible so that it softens when heated). In yet another embodiment, the heat responsive component is a thermoplastic material.

Referring generally to Figure 4, an embodiment utilizing a tri-layer tape will now be described. While dimensional information is provided, it is to be understood that tapes of other layer configurations, sizes, thicknesses, and materials are also contemplated to be within the scope of the invention.

Layers 46, 48 are comprised of a CTBN (Carboxyl Terminated Acrylonitrile-Butadiene) modified epoxy resin formed into layers approximately .0005 inches thick. The resulting adhesive is a thermoset material that laminates at approximately 100 deg C. Complete crosslinking of the material occurs during a higher post-cure temperature as further described herein. The intermediate layer is preferably a polyimide carrier film such as UPILEX® (commercially available from UBE Industries Ltd) or KAPTON® (available from Dupont). In one embodiment, the carrier layer 50 is approximately .002 inches thick. The tri-layer tape as described herein was developed per Applicant's specifications and is presently produced by Ablestik Electronic Materials & Adhesives under part number RP444-3.

Having described the substrate 12, die 10, and adhesive tape 40, a method for attaching the die to the substrate will now be described. The order of the steps may be rearranged to some degree to better accommodate manufacturing processes. Similarly, the processing temperatures, times, and cures discussed herein may be modified to better suite a particular application. Finally, while the curing methods described are temperature processes, other curing methods (e.g., radiation) are also within the scope of the invention.

The method makes reference to various manufacturing "stations" that accomplish specific tasks. These stations are common and well known in the art and are thus perceived to require no detailed explanation. However, the particular step accomplished by each station is described in sufficient detail to enable one of skill in the art to practice the invention.

With reference to Figure 5, the substrate 12 is placed on an automated conveyor system with the first side 24 facing downwardly. The automated machinery then indexes the substrate 12 to a tape punch station. As shown in Figure 5a, the tape 40 is punched into two strips and the first side 42 is pressed against the die attach area 26 of the substrate 12. The tape 40 is heated momentarily to complete the lamination process. The heat applied is generally below that required to crosslink or set the adhesive. In one embodiment, pressure and 100 deg C heat are applied for 100 ms.

Referring now to Figure 5b, the substrate 12 is indexed to the die attach station where the die 10 is brought from beneath the substrate and the die face 14 is placed against the second side 44 of the tape. The die 10 is then pressed against the die attach area 26 with the tape 40 sandwiched therebetween. Once again, the adhesive is activated by heat and pressure. In one embodiment, pressure and 100 deg C heat is applied for 100 ms to laminate the tape 40 to the die 10. At this point, the die is physically attached to the PCB substrate 12. Unlike paste attachment, the

5 tape 40 will not bleed during lamination. Additionally, because the tape thickness is  
easily controlled during manufacture, bond line thickness is more easily controlled.  
Finally, the adhesive tape 40 permits the attachment of the die 10 without having to  
invert the substrate 12 as required with paste applications.

10 Referring now to Figures 5c, the substrate 12 and die 10 are then indexed to  
a wire bonding station wherein the bond pads 16 on the die face 14 are connected to  
the connection pads 30 on the substrate 12 with bond wires 38 passing through the  
aperture 32. Wire bonding can be accomplished with a wire bonder and  
conventional wire bonding methods. While wire bonding is the preferred method  
15 for electrically connecting the die to the substrate, other connection methods (e.g.,  
mechanical, soldered) may also be employed.

20 Next, as shown in Figure 5d, an encapsulating material 52 is applied to the  
second side 28 of the PCB 12 in the wire bond area. The encapsulating material 52  
covers the aperture 32, bond wires 38, connection pads 30 and a portion of the die  
face 14. The encapsulant 52 is preferably a glob-top material that adequately  
protects the bond pads and wire bonds without interfering with other components.  
The glob-top 52 does not appreciably increase the volume of the complete  
25 semiconductor package. It may be an epoxy, silicone or other commercially  
available material suitable for such purposes. The glob-top 52 may be applied by  
conventional methods such as dispensing the material from a needle apparatus  
directly over the wire bond area. In one embodiment, the glob-top is cured for 30  
minutes at 150 deg C.

25 The substrate 12 is then flipped and a glob top 54 is applied to the perimeter  
of the back side (i.e., the side opposite face 14) of die 10 as shown in Figure 5e. The  
substrate 12 and die 10 then enter a post cure process. In one embodiment, the post  
cure is a two-step cure consisting of one hour at 110 deg C followed by one hour at

165 deg C. The post cure operation ensures proper evaporation of all solvents within the glob-top materials 52, 54. Additionally, the cure sets the adhesive layers 46, 48.

At the completion of the final cure, the substrate 12 with its attached die 10 may be sheared to form individually CSPs or plastic BGA (PBGA) packages 56 (see generally Figure 5f). The substrate 12 may be sheared along a line 58 between slots 33 as shown in Figure 2. The singular package 56 is then ready for attachment to other components.

Referring to Figure 5f, the package 56 of the present invention is shown just prior to attachment with a receiving component 60 such as another PCB. To attach the BGA package 56, the BGA solder balls 36 are added on the second side 28 of the substrate 12 and disposed at a height greater than that of the glob-top 52. Thus, the BGA solder balls 36 may contact the receiving substrate 60 without interference from the glob-top 52. To mount the singular BGA package 56 to the receiving component 60, it must first be accurately positioned relative to the component. The package 56 is then pressed against the receiving component 60 until the solder balls 36 contact the mating contacts on the component 60. The assembly may be heated until the solder balls begin to liquefy, thus securing the BGA package 56 to the component 60.

The receiving component 60 in one embodiment is a memory component as shown in Figure 6. The memory component 60 may comprise one or more of the BGA packages 56. The memory component 60 may be incorporated into an electronic device 62 which may incorporate a processor 64.

In an alternative embodiment, the thermosetting adhesive is a B-stageable material. A B-stageable material is actually a thermosetting material that is "re-meltable." That is, it has a first solid phase followed by a rubbery stage at elevated temperature, followed by yet another solid phase at an even higher temperature. The transition from the rubbery stage to the second solid phase is thermosetting.

However, prior to that, the material behaves similarly to a thermoplastic material. Thus, such a material would permit low lamination temperatures while providing high thermal stability.

While the adhesive tape of the present invention has been described as a heat and pressure activated thermoset material, other materials are also contemplated. For example, in another embodiment, each adhesive layer is formed of a pressure sensitive material. Pressure activated adhesives are particularly advantageous in eliminating bond line stress due to coefficient of thermal expansion (CTE) mismatch between the adhesive and the adherents. With temperature activated adhesives, CTE mismatch causes stress at the bond line during lamination because of the different expansion rates of the materials. By using a pressure activated adhesive, no heat is required for lamination. Thus, CTE mismatch is not an issue. By carefully selecting the pressure activated adhesive used, thermal bond line stress can also be minimized during subsequent temperature processing (e.g., wire bonding).

In yet another embodiment, the adhesive tape 40 is a hybrid between a thermoplastic and thermoset material. Unlike the thermoset material, the thermoplastic material is capable of being softened by increases in temperature and hardened by decreases in temperature. Thermoplastic tapes are currently available for LOC applications. This tape is typically a polyimide material requiring temperature processing in excess of 325 deg C. Accordingly, such tapes are ill-suited for use with organic substrates. However, a hybrid thermoplastic tape having a thermoset component therein is considered to fall within the scope of the present invention. The thermoset component of the tape is a material having a low thermal processing requirement. That is, the glass transition temperature (Tg) of the thermoset component is low, allowing the tape to laminate at low or ambient temperature. In one embodiment, the thermoset component has a Tg of approximately 30 deg C. The thermoplastic component of the tape, on the other hand, comprises a high Tg material providing high thermal stability for the

5

subsequent wire bonding and solder reflow operations. Accordingly, the hybrid tape would compromise the high Tg and low Tg characteristics in order to satisfy the competing requirements of the BGA substrate (i.e., low lamination temperature and high thermal stability). Currently available tapes do not address such competing requirements.

10

Thus, an improved method of mounting a semiconductor die to an organic substrate and an improved CSP are described herein. The tape used to mount the die to the substrate addresses many of the problems encountered with conventional paste attachment methods including but not limited to, elimination of resin bleed, improved bond line control, less die face damage due to glob-top filler particles, broader selection of available fillers, and improved in-line processing.

15

Preferred embodiments of the present invention are described above. Those skilled in the art will recognize that many embodiments are possible within the scope of the invention. Variations and modifications of the various parts and assemblies can certainly be made and still fall within the scope of the invention. Thus, the invention is limited only by the following claims, and equivalents thereto.